IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Patent of:

PECONE

Patent No.: 7,062,591

Issued: June 13, 2006

Atty. File No.: 4430-29

For: "CONTROLLER DATA SHARING USING A MODULAR DMA ARCHITECTURE"

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PTO MISTAKE (37 CFR 1.322(a))

CERTIFICATE OF MAILING

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450 ON _____.

SHERIDAN ROSS P.C.

BY: _____

Attn: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is a request for a Certificate of Correction for PTO Mistake under 37 CFR 1.322(a). Attached in duplicate is Form PTO 1050. As evidenced by the attached documents Exhibit A and Exhibit B, the above-referenced patent issued without the amendments made by the Applicant on November 2, 2005 and accepted by the United States Patent and Trademark Office on January 25, 2006.

Exhibit A is a copy of a Request for Continued Examination filed November 2, 2005 including the concurrently filed submission required under 37 C.F.R. §1.114. Amendment to Claims 11-14 and 20 were made in an Amendment and Response After Final submitted on October 11, 2005. These amendments were not considered to place the application in condition for allowance and, as a result, were not entered. The Amendment and Response was again submitted along with a Request for Continued Examination on November 2, 2005. A copy of this submission is included with this paper as Exhibit A. This Request for Continued Examination was timely and complied with the requirement of 37 C.F.R. §1.114.

Exhibit B is a copy of a Notice of Allowance and Fee(s) Due issued by the United States Patent and Trademark Office on January 25, 2006. Exhibit B indicates that the amendments to Claims 11-14 and 20 submitted on November 2, 2005 were entered by the United States Patent and Trademark Office.

Beginning on page 2 of the Amendment and Response filed on November 2, 2005, amendments were properly made to Claims 11-14 and 20. Regrettably, these amendments were not included in the issued patent. Accordingly, a Certificate of Correction is respectfully requested to correct this mistake. The attached Form 1050 contains the amendments made to Claims 11-14 and 20 in the format suggested by MPEP §1485.

Respectfully submitted,

SHERIDAN ROSS P.C.

By: _____

Dennis J. Dupray
Registration No. 46,299
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
(303) 863-9700

Date: July 19, 2006

PTO/SB/44 (04-04)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,062,591

DATED : September 28, 2001

INVENTOR(S) : Victor Key Pecone

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 15, line 41, cancel the text beginning with "11. A method for sharing data" to and ending "memory modules." In column 15, line 56 and insert the following claim:

11. A method for sharing data between a first controller memory module and a second controller memory module, comprising:

providing a first shared path in a first channel interface module (CIM), wherein the shared path includes a switchable component for determining which data is to be routed over the shared path;

wherein the first shared path is included on a data path between the first and second controller memory modules;

a direct memory access engine for each of said first and second controller memory modules; and

transferring first data between said first controller memory module and said second controller memory module using said direct memory access engine for at least one of the first and second controller memory modules, wherein said switchable component provides passage of said first data over said first shared path between the first and second controller memory modules.

MAILING ADDRESS OF SENDER:

DENNIS J. DUPRAY
SHERIDAN ROSS P.C.
1560 BROADWAY
SUITE 1200
DENVER, COLORADO 80202-5141

PATENT NO. 7,062,591

No. of additional copies

PTO/SB/44 (04-04)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,062,591

DATED : September 28, 2001

INVENTOR(S) : Victor Key Pecone

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 15, line 57, cancel the text beginning with "12. The method of claim 11, further comprising:" to and ending "shared path." In column 15, line 64 and insert the following claim:

12. The method of Claim 11, further comprising:

providing a second shared path in a second channel interface module;

wherein the second shared path is included on a data path between the first and second controller memory modules, and the second shared path includes a second switchable component for determining which data is to be routed over the second shared path; and

transferring second data between said first controller memory module and said second controller memory module using said direct memory access engine in the first controller memory module and another direct memory access engine in the second controller memory module, wherein the second data passes through said second shared path.

MAILING ADDRESS OF SENDER:

DENNIS J. DUPRAY
SHERIDAN ROSS P.C.
1560 BROADWAY
SUITE 1200
DENVER, COLORADO 80202-5141

PATENT NO. 7,062,591

No. of additional copies

PTO/SB/44 (04-04)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,062,591

DATED : September 28, 2001

INVENTOR(S) : Victor Key Pecone

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 15, line 65, cancel the text beginning with "11. The method of claim 11, further comprising:" to and ending "of transferring." In column 16, line 3 and insert the following claim:

13. The method of Claim 11, further comprising:

connecting said first channel interface module to both said first and second controller memory modules via a passive backplane, wherein the first data passes through the passive backplane during said step of transferring.

MAILING ADDRESS OF SENDER:

DENNIS J. DUPRAY
SHERIDAN ROSS P.C.
1560 BROADWAY
SUITE 1200
DENVER, COLORADO 80202-5141

PATENT NO. 7,062,591

No. of additional copies

PTO/SB/44 (04-04)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,062,591

DATED : September 28, 2001

INVENTOR(S) : Victor Key Pecone

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 16, line 4, cancel the text beginning with "14. An apparatus for sharing data" to and ending "shared path." In column 16, line 22 and insert the following claim:

14. An apparatus for sharing data between a first controller memory module and a second controller memory module, wherein each of the first and second controller memory modules is for controlling communication of storage data between one or more host computers and one or more storage devices, comprising:

at least a first channel interface module having a first shared path, wherein the shared path has a switchable component, operably associated therewith, for selecting which data is to be routed on the shared path;

a first controller memory module including a first direct memory access engine;

a second controller memory module including a second direct memory access engine;

wherein the first channel interface module is directed by at least one of the first and second controller memory modules to communicate with a first of the host computers and a first of the data storage devices, so that the first channel interface module is operational for sending and receiving storage data between the first host computer and the first storage device;

a communications interface to permit direct communications between said first and second controller memory modules; wherein data is transferred between said first and second controller memory modules using at least one of said first and second direct memory access engines, and using the switchable component, and wherein the direct communications are not routed through the first host computer.

MAILING ADDRESS OF SENDER:

DENNIS J. DUPRAY
SHERIDAN ROSS P.C.
1560 BROADWAY, SUITE 1200
DENVER, COLORADO 80202-5141

PATENT NO. 7,062,591

No. of additional copies

PTO/SB/44 (04-04)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,062,591

DATED : September 28, 2001

INVENTOR(S) : Victor Key Pecone

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 20, line 2 "clannel" should read --channel--.

MAILING ADDRESS OF SENDER:

DENNIS J. DUPRAY
SHERIDAN ROSS P.C.
1560 BROADWAY
SUITE 1200
DENVER, COLORADO 80202-5141

PATENT NO. 7,062,591

No. of additional copies

EXHIBIT A

EXHIBIT A

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL		
Address to: **Mail Stop RCE** **Commissioner for Patents** **P.O. Box 1450** **Alexandria, VA 22313-1450**	Application No.	09/967,126
	Filing Date	September 28, 2001
	First Named Inventor	Victor Key Pecone
	Art Unit	2112
	Examiner	VO, Tim T.
	Attorney Docket No.	4430-29
	Express Mail No.	EV655363519US

This is a Request for Continued Examination (RCE) under 37 C.F.R. §1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application.

1. **Submission required under 37 C.F.R. § 1.114**. Note: If the RCE is proper, any previously-filed, unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendments.

   a. ☒ Previously submitted. If a final Office Action is outstanding, any amendments filed after the final Office Action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on

      ii. ☒ Other Amendment and Response filed October 11, 2005.

   b. ☒ Enclosed

      i. ☒ Copy of Amendment and Response previously filed on October 11, 2005.

      ii. ☐ Affidavit(s)/Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. **Miscellaneous**

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. *(Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(i) required).*

   b. ☐ Other _____

3. **Fees**. The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 19-1970. I have enclosed a duplicate copy of this sheet

      i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)

      ii. ☐ Extension of time fee *(37 C.F.R. §§ 1.136 and 1.17)*

      iii. ☐ Other _____

   b. ☒ Check in the amount of $ $395.00 enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed).

Signature		Date	Nov. 1, 2005
Name (Print/Type)	DENNIS J. DUPRAY	Registration No. (Attorney/Agent	46,299

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	09/967,126
Applicant	:	PECONE
Filed:	:	September 28, 2001
Group Art Unit	:	2112
Examiner	:	VO, Tim T.
Docket No.	:	4430-29
Customer No.	:	4944
Title	:	"CONTROLLER DATA SHARING USING MODULAR DMA ARCHITECTURE"

"EXPRESS MAIL" MAILING LABEL NUMBER: EV655362703US

DATE OF DEPOSIT: October 14, 2005

I HEREBY CERTIFY THAT THIS PAPER OR FEE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE VIA "EXPRESS MAIL" ADDRESSED TO THE COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450.

TYPED OR PRINTED NAME: Chasity C. Rossum

SIGNATURE

Mail Stop: Amendments
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE TO OFFICE ACTION DATED AUGUST 9, 2005

Dear Sir:

Applicant submits this Amendment and Response to address the Office Action having a mailing date of August 9, 2005.

Please amend the above-identified patent application as follows:

AMENDMENTS TO CLAIMS

11. (Currently Amended) A method for sharing data between a first controller memory module and a second controller memory module, comprising:

providing a first shared path in a first channel interface module (CIM), wherein the shared path ~~has~~ includes a switchable component for determining which data is to be routed over the shared path;

wherein the first shared path is included on a data path between the first and second controller memory modules;

a direct memory access engine for each of said first and second controller memory modules; and

transferring first data between said first controller memory module and said second controller memory module using said direct memory access engine for at least one of the first and second controller memory modules, wherein said switchable component provides passage of said first data over said first shared path between the first and second controller memory modules.

12. (Currently Amended) The method of Claim 11, further comprising:

providing a second shared path in a second channel interface module;

wherein the second shared path is included on a data path between the first and second controller memory modules, and the second shared path includes a second switchable component for determining which data is to be routed over the second shared path; and

transferring second data between said first controller memory module and said second controller memory module using ~~each of~~ said direct memory access engine[[s]] in the first controller memory module and another direct memory access engine in the second controller memory module, wherein the second data passes through said second shared path.

13. (Currently Amended) The method of Claim 11, further comprising:

connecting said first ~~and second~~ channel interface module[[s]] ~~and~~ to both said first and second controller memory modules ~~to~~ via a passive backplane, wherein the first data passes through the passive backplane during said step of transferring.

14. (Currently Amended) An apparatus for sharing data between a first controller memory module and a second controller memory module, wherein each of the first and second controller memory modules is for controlling communication of storage data between one or more host computers and one or more storage devices, comprising:

at least a first channel interface module having a first shared path, wherein the shared path has a switchable component, operably associated therewith, for selecting which data is to be routed on the shared path;

a first controller memory module including a first direct memory access engine;

a second controller memory module including a second direct memory access engine; ~~and~~

wherein the first channel interface module is directed by at least one of the first and second controller memory modules to communicate with a first of the host computers and a first of the data storage devices, so that the first channel interface module is operational for sending and receiving storage data between the first host computer and the first storage device;

a communications interface to permit direct communications between said first and second controller memory modules; wherein data is transferred between said first and second controller memory modules using at least one of said first and second direct memory access engines, and using the switchable component ~~of said first shared path,~~ and wherein the direct communications are not routed through the first host computer.

15. (Previously Presented) The apparatus of Claim 14, further including:

a second channel interface module having a second shared path, wherein the second shared path has a second switchable component, operably associated therewith, for determining which data is to be routed over the second shared path;

wherein said second switchable component provides passage of second data over said second shared path between the first and second controller memory modules using each of said first and second direct memory access engines.

16. (Previously Presented) The apparatus of Claim 14, wherein:

said communications interface includes a passive backplane.

17. (Previously Presented) The apparatus of Claim 16, wherein:

said passive backplane includes at least first and second peripheral component interconnect (PCIX) buses.

18. (Previously Presented) The method of Claim 11, wherein the first shared path transmits the first data between the direct memory access engines of the first and second controller memory modules.

19. (Previously Presented) The method of Claim 11, further including providing a plurality of data buses, wherein each of said data buses is operably connected between a first one of the direct memory access engines and the first shared path for communicating the first data.

20. (Currently Amended) The method of Claim 19, further including:

providing a second shared path in a second ~~elannel~~ channel interface module;

transferring second data between said first controller memory module and said second controller memory module using each of said direct memory access engines, wherein the second data passes through said second shared path;

a second plurality of said data buses, wherein each of the second plurality of said data buses is operably connected between a second one of the direct memory access engines and the second shared path for communicating the second data.

Please cancel Claim 21

22. (Previously Presented) The method of Claim 13, wherein the passive backplane includes two data busses for communicating with each of the first and second controller memory modules.

REMARKS

Applicant's representatives present the claim amendments herein after final rejection.

Regarding Claim 11, the Examiner states that Smith teaches a method for sharing data between a first controller memory module and a second controller memory module, comprising providing a first shared path in a first channel interface module, wherein the shared path has a switchable component for determining which data is to be routed over the shared part. The following relate to the above recited components:

(a) The first and second controller memory modules apparently are asserted by the Examiner to be all the components 215-280. Thus, the Examiner is apparently asserting that the first controller memory module is substantially the entire mobile computer 110, and the second controller memory module is the components: PCI-to-PCI bridge 260, secondary bus 262, PCI-to-ISA bridge 270, and slave DMA controller 280. However, Applicant's representatives are not clear as to which components the Examiner is asserting as the first controller memory module, and which components the Examiner is asserting as the second controller memory module.

(b) The first shared path (in a first channel interface module) is identified in one portion of the Examiner's response as the primary PCI bus 240 and the secondary bus 262. However, an alternative interpretation of the Examiner's comments might be that the first shared path is the primary PCI bus 240, and the first channel interface module is the secondary PCI bus 262. Since this primary PCI bus 240 is not ***in*** the secondary bus 262, this alternative interpretation appears inappropriate. However, in another portion of the Examiner's response the first shared path is apparently identified as: the primary PCI bus 240, the secondary bus 262, the bridge 260.

(c) The Examiner does not identify a component(s) of Smith corresponding to the "first channel interface module". However, since Claim 11 recites that the "first shared path" is ***in*** the first channel interface, the first channel interface must presumably at least include the components identified by one of the Examiner's interpretations of the "first shared path". However, it is unclear what Examiner intends the "first channel interface module" to correspond to in Smith.

(d) The Examiner further identifies the "switchable component", apparently, as Smith's central DMA 215, and the Examiner cites column 8, lines 20-30 to substantiate his assertion that the DMA 215 can be the switchable component. For completeness, this Smith passage is recited here:

> "Once the slave DMA controller 280 has transmitted the appropriate data to the central DMA controller 215, control passes to a sub-method block 340 wherein the central DMA controller 215, under the direction of the state machine 217, transfers the appropriate channel data, including the channel number, the base address and count data, and the data to be stored in the mode register, to the slave DMA controller 280. This channel data is transmitted to the slave DMA controller 280 via the primary PCI bus 240, the PCI-to-PCI bridge 260, the secondary PCI bus 262, and the PCI-to-ISA bridge 270."

Thus, since Smith's central DMA controller 215 is not part of the Examiner's identified "first shared path", the Examiner is presumably interpreting the word "has" in the Claim 11 phrase "the shared path ***has*** a switchable component for determining which data is to be routed over the shared path" as being equivalent to "associated therewith".

Applicant's representatives have attempted to address the Examiner's rejection of Claim 11 as follows. Claim 11 has been amended to recite that: (a) the first shared path **includes** the switchable component, and (b) the first shared path is included on a data path between the first and second controller memory modules. Accordingly, when (a) and (b) are taken together, it is believed that neither of the Smith DMAs 215, 280 can be interpreted as including the switchable component. Thus, it is believed that the Examiner's rejection of Claim 11 is overcome. However, in the event that the Examiner disagrees with the above reasoning, it is respectfully requested that the Examiner more clearly identify in Smith the features that are asserted as corresponding to components and limitations of Claim 11.

Regarding Claim 12, the Examiner states that Smith teaches providing a second shared path in a second channel interface module wherein the second shared path is (as best as can be understood) is identified as the DMA request line 298. However, it is believed that the Examiner did not identify the "second channel interface module". Accordingly, it is

respectfully requested that the Examiner explicitly identify the "second channel interface module". Additionally, the Examiner states that Smith teaches transferring "second data" between the first and second controller memory modules using each of the direct memory access engines, wherein the second data passes through the second shared path. However, the Examiner identifies the second shared path in this latter context as being "bus 216, DMA 212-213". It is assumed that "bus 216, DMA 212-213" was stated in error by the Examiner since Fig. 2 of Smith has no bus 216, no DMA 212, and no DMA 213. Additionally, there is no 212, 213 nor 216 disclosed in Smith's specification. Thus, it is assumed that the Examiner's (apparent) first identification of the "second shared path", as request line 298, is what is intended.

Applicant's representatives have attempted to address the Examiner's rejection of Claim 12 as follows. Claim 12 has been amended to recite that: (a) the second shared path is included on a data path between the first and second controller memory modules, and (b) the second shared path includes a second switchable component for determining which data is to be routed over the second shared path. Assuming the first and second controller memory modules are as the Examiner identified them in Claim 11 (or as best as can be determined), it is believed that the combination of the limitations (a) and (b) overcomes the Examiner's rejection of Claim 12. In particular, DMA request line 298 does not include a "second switchable component". Moreover, note that this limitation was recited in previously entered Claim 21.

Regarding Claim 13, the Examiner states that Smith teaches connecting the first and second channel interface modules and the first and second controller memory modules to a passive backplane. The Examiner's justification for this assertion is "see figure 2". However, it is respectfully submitted that figure 2 of Smith does not teach or suggest using a passive backplane as this term is used in the art. As described in the previous Amendment and Response provided to the Examiner, a passive backplane is described in the following definition of "backplane":

> (bak′plān) **(n.)** A circuit board containing sockets into which other circuit boards can be plugged in. In the context of PCs, the term backplane refers to the large circuit board that contains sockets for expansion cards.

> Backplanes are often described as being either *active* or ***passive.*** Active backplanes contain, in addition to the sockets, logical circuitry that performs computing functions. In contrast, passive backplanes contain almost no computing circuitry.
>
> Traditionally, most PCs have used active backplanes. Indeed, the terms *motherboard* and *backplane* have been synonymous. Recently, though, there has been a move toward **passive backplanes**, with the active components such as the CPU inserted on an additional card. Passive backplanes make it easier to repair faulty components and to upgrade to new components.
>
> http://www.webopedia.com/TERM/B/backplane.html

Another description of "passive backplane" is as follows:

> All the active circuitry that [in] is normally found on an "active" PC motherboard (such as the CPU) is moved to a plug-in card. The new motherboard has nothing on it other than connectors, and is referred to as a **passive backplane**. The chance of a passive backplane failing is very low. Also referred to as "slot card" technology. (8/97)
>
> http://topcc.org/glossary/glossp.htm

Applicant's representatives can, if the Examiner desires, supply numerous other similar descriptions of passive backplanes. As best as can be understood, presumably the Examiner is suggesting that Smith's docketing interface 255 is a passive backplane. However, it is believed that no where in Smith is there any teaching or suggestion of the docketing interface 255 being a passive backplane. In fact, the only description of the docketing interface 255 is as follows:

> "The notebook computer 110 engages with the docking station 120 (also shown in FIG. 2 as enclosed within a dashed line) via a docking interface 255. The docking interface 255 preferably comprises an electrical connector which electrically connects the notebook computer 110 to the docking station 120. A PCI-to-PCI bridge 260 within the docking station 120 connects to the docking

> interface 255 to provide an interface between the primary PCI bus 240 within the notebook computer 110 and a secondary PCI bus 262 within the docking station 120. The PCI-to-PCI bridge 260 preferably includes a repeater as well as other connector and conventional interface circuitry to provide for error free communication between the primary PCI bus 240 and the secondary PCI bus 262. The PCI-to-PCI bridge 260 is preferably constructed in accordance with the specifications laid out in revision 1.0 of the PCI-to-PCI bridge architecture specification available from PCI special interest group, N/SHS3-15A, 5200 N.E. Elam Young Parkway, Hillsboro, Oreg. 97124-6497." (Smith, col.5, ln. 57 through col. 6, ln. 8)

Accordingly, if the Examiner still persists in asserting that Smith's docketing interface 255 is a passive backplane, then it is respectfully requested that the Examiner provide substantiation for such an assumption.

Additionally, since the Examiner has not identified the "first channel interface module" in Smith, it is respectfully requested that if the Examiner persists in rejecting Claim 13, that the Examiner identify the "first channel interface module" in manner consistent with the limitations of Claim 13.

Regarding Claim 14, this claim has been amended to recite that:

(a) Each of the first and second controller memory modules is for controlling communication of storage data between one or more host computers and one or more storage devices;

(b) "The first channel interface module is directed by at least one of the first and second controller memory modules to communicate with a first of the host computers and a first of the data storage devices, so that the first channel interface module is operational for sending and receiving storage data between the first host computer and the first storage device"; and

(c) "Direct communications" via a "communications interface" is permitted between the first and second controller memory modules wherein the "direct communications" are not routed through the first host computer.

It is believed that Claim 14 now overcomes the Examiner's rejections, and accordingly, Claim 14 is now in condition for allowance.

Since Claims 15 through 22 are dependent upon at least one of the allowable Claims 11 through 14, it is believed that Claims 15 through 22 are now also in condition for allowance.

Since all claims are now believed to be in condition for allowance, Applicant's representatives request reconsideration of the present application, and prompt allowance thereof. It is believed that no fees are due with this transmittal, but in the event that any fees are due, please charge Deposit Account No. 19-1970. Since this transmittal is timely filed within the allotted time for an Advisory Action, it is requested that the Examiner contact the undersigned as soon as possible regarding whether the Examiner will allow the present application, and/or for determining how best to put the present application in condition for allowance.

Respectfully submitted

SHERIDAN ROSS P.C.

By: _____

Dennis J. Dupray
Registration No. 46,299
1560 Broadway, Suite 1200
Denver, Colorado 80202
Phone: 303-863-9700

Date: Oct. 11 2005

J:\4430\-29\To Be Filed\AMD-02-Rsp to 8-9-05 OA.doc

28257

SHERIDAN ROSS P.C.
PROFESSIONAL ACCOUNT
ATTORNEYS AND COUNSELORS AT LAW
1560 BROADWAY, SUITE 1200
DENVER, COLORADO 80202
(303) 863-9700

WELLS FARGO BANK, N.A.
DENVER
DENVER, CO 80274
23-7-1020

DATE	CHECK NO.	CHECK AMOUNT
11/01/05	28257	*$395.00*

THREE HUNDRED NINETY FIVE AND 00/100 DOLLARS

PAY TO THE ORDER OF COMMISSIONER OF PATENTS AND TRADEMARKS

U.S. DOLLARS
VOID AFTER 180 DAYS
SHERIDAN ROSS AUTHORIZED SIGNATURE

⑈028257⑈ ⑆102000076⑆ 2016571798⑈

Security Features Included. Details on back.

SHERIDAN ROSS

VENDOR NO. VENDOR NAME 28257

TRANSACTION DATE	REFERENCE	GROSS AMOUNT	DEDUCTION	NET AMOUNT
11/01/05	OPER-CCR	Request for Continued Examination 4430-29	1122000	395.00

CHECK DATE	CHECK NO.	TOTAL GROSS	TOTAL DEDUCTION	CHECK AMOUNT
11/01/05	28257			395.00

Customer Copy
Label 11-F, April 2004

EV 655363519 US

EXPRES MAIL
UNITED STATES POSTAL SERVICE®

Post Office To Addressee

ORIGIN (POSTAL SERVICE USE ONLY)

PO ZIP Code: 80202	Day of Delivery: ☐ Next ☐ 2nd ☐ 2nd Del. Day	Postage: $
Date Accepted: 11 2 05 (Mo. Day Year)	Scheduled Date of Delivery: Month 11 Day 4	Return Receipt Fee: $
Time Accepted: 6:42 ☐ AM ☒ PM	Scheduled Time of Delivery: ☑ Noon ☐ 3 PM	COD Fee: $ / Insurance Fee: $
Flat Rate ☐ or Weight: lbs. 3 ozs.	Military: ☐ 2nd Day ☐ 3rd Day	Total Postage & Fees: $ 13.65
	Int'l Alpha Country Code	Acceptance Emp. Initials

DELIVERY (POSTAL USE ONLY)

Delivery Attempt Mo. Day	Time ☐ AM ☐ PM	Employee Signature
Delivery Attempt Mo. Day	Time ☐ AM ☐ PM	Employee Signature
Delivery Date Mo. Day	Time ☐ AM ☐ PM	Employee Signature

DENVER DOWNTOWN STATION NOV 2 2005 USPS 80202

☐ WAIVER OF SIGNATURE *(Domestic Mail Only)* Additional merchandise insurance is void if w[illegible] of signature is requested. I wish delivery to be made without obtaining signature of addressee or addressee's agent (if delivery employee judges that article can be left in secure location) and I authorize that delivery employee's signature constitutes valid proof of delivery.

NO DELIVERY ☐ Weekend ☐ Holiday

Customer Signature

CUSTOMER USE ONLY

METHOD OF PAYMENT:

Express Mail Corporate Acct. No.:

Federal Agency Acct. No. or Postal Service Acct. No.:

FROM: (PLEASE PRINT) PHONE ( )

SHERIDAN ROSS PC
1560 BROADWAY STE 1200
DENVER CO 80202-5143

4430-29 (CCR)

TO: (PLEASE PRINT) PHONE ( )

COMMISSIONER FOR PATENTS
PO BOX 1450
ALEXANDRIA VA 22313-1450

MS RCE

FOR PICKUP OR TRACKING: Visit www.usps.com or Call 1-800-222-1811 EMS

FOR PICKUP OR TRACKING: Visit www.usps.com or Call 1-800-222-1811 EMS

114/A500 F:02 T:23

Initial: CCR BMK (?) Date: 11-2-05

PTO Stamp indicates receipt of: [X] Patent Matter [] Trademark Matter

Application Docket No.: 4430-29

Applicant: PECONE

Title or Mark: "CONTROLLER DATA SHARING USING MODULAR DMA ARCHITECTURE"

Serial/Reg. No.: 09/967,126

Filed/Issued Date: September 28, 2001

[] Certificate of Mailing

[X] Express Mail No.: EV655363519US

[X] Check for $395.00

OIPE IAP15 NOV 02 2005 PATENT & TRADEMARK OFFICE

RECEIVED NOV 11 2005 SHERIDAN, ROSS

____ No. of Pages in Specification

____ No. of Pages in Claims

____ No. of Sheets of Drawings

LIST ALL DOCUMENTS BEING SENT TO PATENT OFFICE:

Request for Continued Examination
Copy of Amendment and Response Previously Filed October 11, 2005

EXHIBIT B

EXHIBIT B

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22442 7590 01/25/2006

SHERIDAN ROSS PC
1560 BROADWAY
SUITE 1200
DENVER, CO 80202

EXAMINER	
VO, TIM T	
ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 01/25/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,126	09/28/2001	Victor Key Pecone	4430-29	4944

TITLE OF INVENTION: CONTROLLER DATA SHARING USING A MODULAR DMA ARCHITECTURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	04/25/2006

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/05) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571) 273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22442 7590 01/25/2006

SHERIDAN ROSS PC
1560 BROADWAY
SUITE 1200
DENVER, CO 80202

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,126	09/28/2001	Victor Key Pecone	4430-29	4944

TITLE OF INVENTION: CONTROLLER DATA SHARING USING A MODULAR DMA ARCHITECTURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	04/25/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
VO, TIM T	2112	710-313000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Notice of Allowability	Application No.	Applicant(s)	
	09/967,126	PECONE, VICTOR KEY	
	Examiner	Art Unit	
	Tim T. Vo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 11/02/05*.

2. ☒ The allowed claim(s) is/are *1-20 and 22*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/23/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Tim T. Vo
Primary Examiner
Art Unit: 2112

Examiner's Statement of Reasons for Allowance

1. Claims 1-20 and 22 are allowable over the prior of records.

2. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 1, 11 and 14 are allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts. As for claim 1, prior art fails to teach at least first and second controller memory modules, connected to the passive backplane, that communicate with the channel interface modules via the passive backplane, and that store and process the storage transferred to and from the channel modules. As for claim 11, prior art fails to teach a first share path in a first channel interface module (CIM), wherein the shared path includes a switchable component for determining which data is to be routed over the shared path. As for claim 14, prior fails to teach wherein the first channel interface module is directed by at least one of the first and second controller memory modules to communicate with a first of the host computers and a first of the data storage device, so that the first channel interface module is operational for sending and receiving storage data between the first host computer and the first storage device.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 571-272-3642. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3672. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/20/06

Tim T. Vo
Primary Examiner
Art Unit 2112

FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 4430-29	SERIAL NO. 09/967,126
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT PECONE	
		FILING DATE September 28, 2001	GROUP ART

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROP.
NL	1	5,345,565	9/6/94	Jibbe et al.	~~395~~	~~325~~	
NL	2	5,530,842	6/25/96	Abraham et al.	~~395~~	~~500~~	
NL	3	5,668,956	9/16/97	Okazawa et al.	~~395~~	~~306~~	
NL	4	6,243,829	6/5/01	Chan	~~714~~	~~7~~	
NL	5	6,272,533	8/7/01	Browne	~~709~~	~~213~~	
NL	6	6,507,581	1/14/03	Sgammato	~~370~~	~~381~~	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION	
							YES	NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

NL	7	Young et al., "A high I/O reconfigurable crossbar switch" (2003) (abstract) 2 pages
NL	8	Landman and Rabaey, "Activity-sensitive architectural power analysis" (1996) (abstract) 5 pages

EXAMINER	DATE CONSIDERED
/Lun Li/	1/20/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,126	09/28/2001	Victor Key Pecone	4430-29	4944

22442 7590 01/25/2006

SHERIDAN ROSS PC
1560 BROADWAY
SUITE 1200
DENVER, CO 80202

EXAMINER	
VO, TIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 01/25/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 806 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 806 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 07/05) Approved for use through 04/30/2007.